

UniSTAC® II PXA255 Full In-Circuit Emulator



- ❑ Supports Intel® PXA255 Applications Processor
- ❑ Supports CPU maximum clock speed
- ❑ Watchpoint®, Sophia's powerful C/C++ source language debugger
- ❑ 64K cycles real-time bus trace and branch trace capability
- ❑ 100 MHz external bus speed supported
- ❑ Thumb® state code debugging in Watchpoint®
- ❑ Hardware breakpoint can be set for address/data/status conditions (2 instruction BPs, 2 data BPs)
- ❑ 64Mbytes SDRAM on dummy target
- ❑ Unlimited software breakpoints
- ❑ Flash memory write capability
- ❑ View/modify internal peripheral and coprocessor registers
- ❑ Performance, Profile, and Coverage measurements
- ❑ USB and LAN host interfaces supported for high-speed communication with host computer

Specifications

Target CPU	Intel® PXA255 Applications Processor
Target/ICE Connection	Sophia ICE connector standard. Optional mBGA256 adapter available.
CPU Clock	CPU maximum internal clock. 100 MHz external bus
Target Vcc	Core: +1.05 ~ 1.5VDC, I/O: 3.3V
Memory and I/O	All memory and I/O space is available to user except 4KB in monitor area
Interrupts	Both internal and external interrupts are available to user
Breakpoints and Break Options	Execution address break options <ul style="list-style-type: none"> • Hardware breakpoints (2 ~ 4 breakpoints available depending on map setting) • Unlimited software breakpoints Other break options <ul style="list-style-type: none"> • Forced break from debug monitor • Break on Write-protect error • Break on Trace-end (specify address/data/status conditions)
ICE Environment Settings	Enable/disable RESET, BOOTSEL 0~ 2 signal from target with key operations
CPA Function	Coverage measurement monitors accesses (hits) within a 64-Kbyte area (specify code fetch/memory read/write)
Reset	Reset the CPU during program execution from debugger or target
Flash Memory	Download to target external Flash memory
Branch Trace	Records Branch instruction history, and trace instructions until break

Emulation Memory	8 Mbytes emulation memory for CS0~CS5 area, 32-bit /16-bit width is supported. Two memory blocks, 128 Kbytes ~ 8 Mbytes size, can be allocated. Write protect memory attribute can be specified. SMROM cannot be allocated for emulation memory
Real-time Trace	<p>Trace Buffer Memory Stores 64K frames real-time bus cycle information</p> <p>Trace Recording Address, data, CPU status, control signals, external</p> <p>Trace Modes</p> <p>Free-run- Continuously records Trace data</p> <p>Point1~5- Triggers on specific point (5 separate trigger points can be defined)</p> <p>OR- Triggers when one of the points is satisfied</p> <p>AND- Triggers when all of the points are satisfied</p> <p>Sequential- 2 sequential levels for Trace recording</p> <p>Sampling- Records trigger cycles only</p> <p>Trigger Point Conditions: The following conditions can be specified when defining trigger points:</p> <p>Address: Specify memory address (Bit-maskable)</p> <p>Data: Specify a data value (Bit-maskable)</p> <p>CPU Status: Specify code fetch/memory read, memory write, memory access</p> <p>Other Trigger Conditions:</p> <ul style="list-style-type: none"> -Trigger on CPU external pin signals (specify low/high) -External Trigger Output
Performance Analyzer	Measures cache hit rate, and number of execution cycle for one target instruction
Limitations	-Uses CPU internal register for Performance measurement

Configuration

The UniSTAC™ II PXA255 Full ICE provides a high level of software debugging and hardware testing from your PC/AT or notebook computer. It is a development tool for designs containing an Intel® PXA255 Application Processor based on Xscale™ Microarchitecture. The UniSTAC-II PXA255 Full ICE connects to Sophia ICE connector on the target without removing target processor, or the probe end can be connected to an mBGA adapter on the target.

Hardware

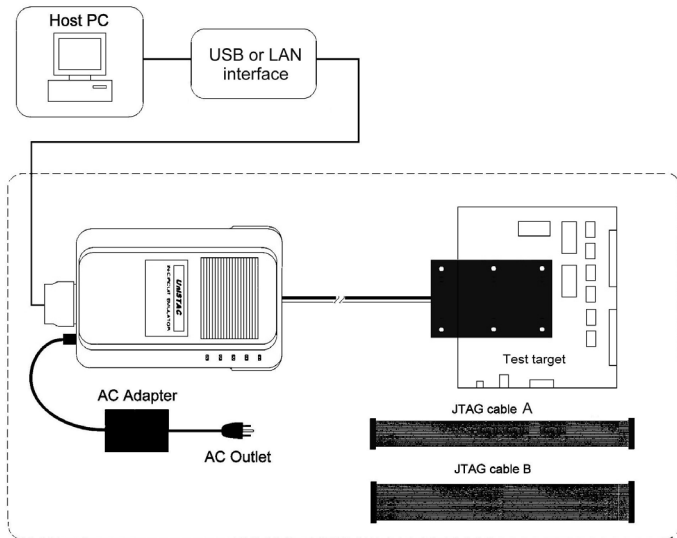
A UniSTAC-II PXA255 Full emulation system consists of the PXA255 Full ICE Probe Set with USB host interface (optional LAN interface available).

Probe Set

The Probe Set consists of the PXA255 Probe Unit, and AC Adapter.

USB and LAN Interface

USB and LAN interface can be used for high-speed communication between the host PC and ICE.



UniSTAC II XScale PXA255 Full ICE

System requirements for Watchpoint® Debugger:

OS: Windows 98/Me/2000/NT/XP
Memory: 32 Mbyte (64 Mbyte recommended)
Hard Disk: 20 Mbyte for installation

Software

Watchpoint®, a high-level language debugger for Windows® 98/Me/NT/2000/XP, is included with PXA255 Probe Set.

Media:

CD-ROM

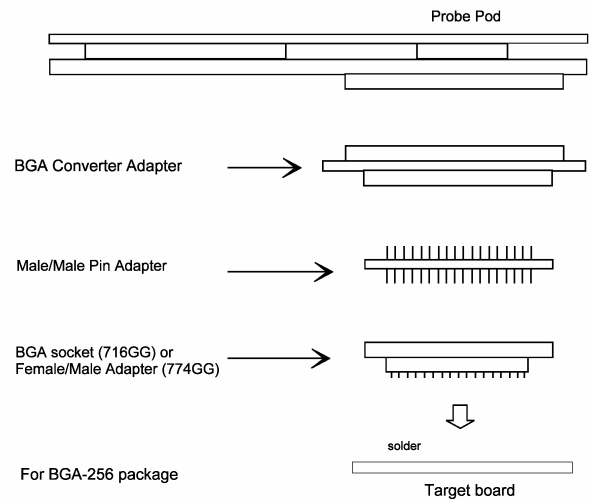
Supported OS

Windows®CE.NET™, Linux, ITRON such as ThreadX

Supported Tool Chains:

Watchpoint supports the following compilers
 Intel® C++ Software Development Tool Suite
 ARM ADS, Realview

Target Connection



BGA-256 connection

Ordering Information

Part No.	Description
UT13002E	Probe Set, UniSTAC II PXA255 Full ICE with USB & LAN interface, and Watchpoint® PXA255 debugger

Package	Adapter/Socket
BGA256 (1 set with 3 types of adapter)	CS2712D PXA250-PB-BGA256-AD
	YY9001 4FHAX256-735G
	YY9001 4FHSB256-774GG or
	YY9001 4FHSB256-716GG

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