

ETM+RTP JTAG Emulator EJ-Debug for TI TMS Automotive



- Works with Code Composer Studio® IDE
- Supports TI TMS series: TMS470, TMS570*
- ARM®/Thumb® state debugging supported
- Set hardware breakpoints on address and status
- Unlimited software breakpoints
- Clear, read and program FLASH
- 512 K-step ETM trace including ETB
- Available ETM trace up to 200MHz clock
- 1.8V up to 3.6V target voltage support
- Perfect for field debugging or maintenance.
 - USB bus powered - No AC adapter required.
 - Pocket sized, 86x101x23mm
- JTAG pod button runs User macro scripts
 - Perfect for hardware test, small run programming and automatic field upgrades.
- Fast USB PC interface.
- EJ-Debug includes Watchpoint® for Windows®

Specifications

Target CPU	TMS470, TMS570* --- ARM cores --- ARM Cortex-R4 TMS570* ARM11 OMAP2430, OMAP2420, OMAPV2230, etc. ARM1156, ARM1136, etc. ARM9 OMAP17xx, OMAP16xx, OMAP15xx, OMAP59xx OMAPV2230, OMAPV1030, OMAP-DM270, OMAP850, OMAP7xx, etc. ARM9TDMI, ARM9TDMI-S, ARM910T, ARM920T, ARM940T ARM9E, ARM946E, ARM966E, ARM922, ARM925, ARM926, etc. ARM7 TMS320, TMS470, etc. OMAP-DM270, OMAP850, OMAP7xx ARM7TDMI, ARM7TDMI-S, ARM710T, ARM720T, ARM740T, etc.	*TMS570 is an additional Option: Check with T.I. for availability.
Clock	200 MHz Maximum CPU clock	
Target Vcc	Target Vcc from +1.8 V to 3.6 V	
Memory & I/O	Entire space is available to the User	
Interrupts	Both internal and external interrupts are available to user	
Breakpoints and Break Options	Hardware breakpoints 2 hardware breakpoints in ARM7 and ARM9 Instruction execution address, memory access, data can be specified. 7 hardware breakpoints(ARM11): Instruction execution address(3 points), memory access(2 points), others(2 points) Unlimited software breakpoints Other break options: Forced break from Debug Monitor Note: ARM7 & 9, Step Over, Step Out, & Run to Cursor functions uses one core hardware breakpoint.	
ETM Trace + ETB Embedded Trace Macro cell	200Mhz clock support 512 K-step trace memory The following conditions can be specified: Set area start and stop trace triggers Time stamp capability, ETB capability	
Flash Memory	JTAG target FLASH read, test, clear and programming functions	

Configuration

Hardware

The EJ-Debug ETM for ARM7/9/11/Cortex system consists of a ARM7/9/11/Cortex JTAG pod with a USB2.0 to PC interface.

Software

Watchpoint®, a high-level language debugger for Windows® Vista*/XP/2000, is included with the EJ-Debug for ARM7/9/11/Cortex.

Media

CD-ROM

Supported Tool Chains

Watchpoint supports the following compilers and OS

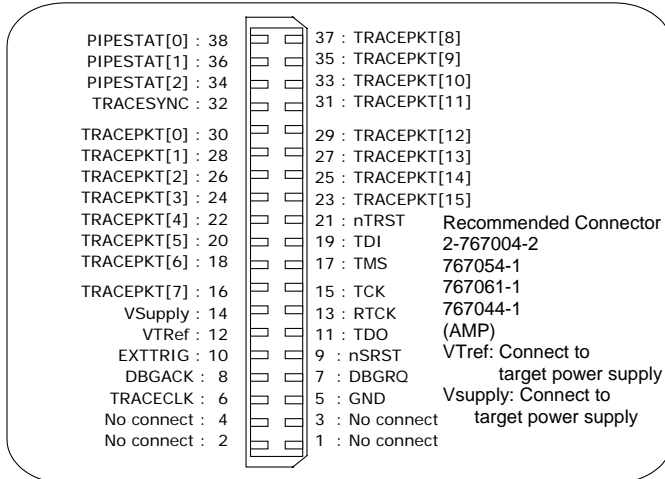
Compilers

TI Code Composer Studio®
 ARM: ADS, SDT, RVCT
 Metaware: High C/C++/EC++ for ARM
 Green Hills: GHS
 GAIO: XCC-V
 GNU:
 IAR: EWARM

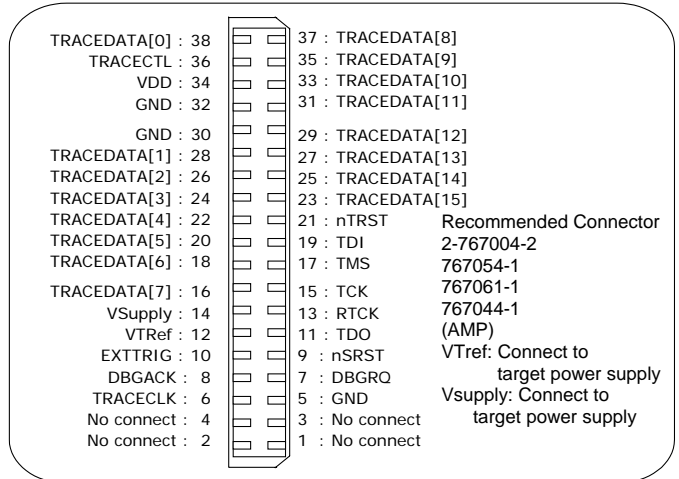
Supported OS

Linux Windows CE™ Symbian OS™
 NORTI G-OS PrKERNEL
 VxWorks ITRON Othe

Target JTAG Connections

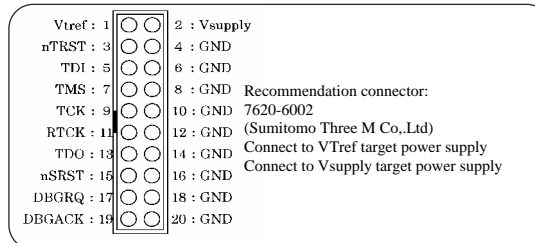


Single ETM Target connector pins for ARM7/9 - Top View



Single ETM connector pins for ARM11 – Top View

JTAG Connector pins – Top View



Ordering Information

Part No.

Description

EJD7204E JTAG Emulator, EJ-Debug ETM for ARM7/9/11 with USB2.0 host interface, and **Watchpoint® debugger**.
 EJD7304E JTAG Emulator, EJ-Debug ETM for ARM7 with USB2.0 host interface, and **Watchpoint® debugger**.
 EJD7824E JTAG Emulator, EJ-Debug ETM for ARM7/9/11/Cortex with USB2.0 host interface, and **Watchpoint® debugger**.

System requirements for Watchpoint® Debugger:

OS	Memory	Hard Disk
Windows XP/2000	64 Mbytes	25 Mbyte for installation
Windows Vista	512 Mbytes	25 Mbyte for installation

Notes:

- * **Vista (32-bit version): driver software update is required.**
 - * **Vista (64-bit version): not supported by current version of Watchpoint.**
 - * **XP (64-bit version): driver software update is required.**
- Earlier versions of Watchpoint do not support Windows Vista.**
An interim version is available now. Please contact your local Rep/Distributor.

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