



EJ-Debug for Xtensa LX Multi Core



- ❑ Supports Tensilica licenced Xtensa LX
- ❑ Debugs multiple Tensilica Xtensa core CPUs at one time^{*1}
- ❑ Supports Tensilica Diamond Standard Processors^{*2}
- ❑ Supports ICE interface specified by Tensilica
- ❑ Supports TIE, FLIX instruction
- ❑ View and modify internal peripheral registers
- ❑ 4 hardware breakpoints (Instruction address: 2 points, Data address: 2 points)
- ❑ Unlimited software breakpoints
- ❑ Download to Flash Memory capability
- ❑ Useful for field debugging or maintenance
 - Powered by USB bus(No AC adapter required)
 - Small size(86mm X 101mm X 23mm)
- ❑ Auto-script execution by BATCH button on the hardware unit
 - perfect use in auto-verification of the target on mass production or for updating new versions
- ❑ USB host interfaces for high-speed communication with host computer
- ❑ Sophia's high-level language debugger, Watchpoint®, is included with all Sophia Systems emulators (Windows®98/Me/2000/XP platforms)
- ❑ Supports all RTOS compliant with TOPPERS μITRON(Ver4.0) specifications.

Specifications

Target CPU	T1020, T1030, T1040, T1050, Xtensa LX, Xtensa6 ^{*3} Diamond Standard Processors (Supports the ASIC with the on-chip debugging interface)
Target Vcc	Vcc= +1.8 V to 3.6 V
Memory and I/O	Entire space is available to user
Interrupts	Both internal and external interrupts are available to user
Breakpoints and Break Options	Execution address break options: <ul style="list-style-type: none"> • Hardware breakpoints (Instruction address: 2 points, Data address: 2 points)* <ul style="list-style-type: none"> Execution instruction address and memory access can be specified. * The number of hardware breakpoints (BP) will be specified when configuring the CPU. * Upon configuring the CPU, 2 instruction executions and 2 data access addresses must be specified. • Unlimited software breakpoints Other break options: Forced break from the debugger
Flash Memory	Download to target external Flash memory

*Note1: Max 10 CPUs can be debugged at the same time.

But the CPU internal configuration or PC environment may have an effect on the number of CPUs being debugged.

*Note2: Supports the ASIC that includes Diamond Standard Processors and the on-chip debugging interface.

*Note3: The EJ-Debug for Xtensa LX supports Xtensa6, Diamond Standard Processors, but does not support the MMU capability of these CPUs.

*Note4: Regarding the trace feature, Sophia's debugger can support the XtensaLX feature that installs the trace feature. Please contact us about more details about the trace feature.

Configuration

The EJ-Debug for Xtensa LX Multi Core provides a high level of software debugging from your PC/AT or notebook computer.

Hardware

A EJ-Debug for XtensaLX Multi Core system consists of the XtensaLX Probe Set with USB host interface.
(EJ-Debug for Xtensa LX Multi Core can not be used for other CPUs)

Software

Watchpoint®, a high-level language debugger for Windows®98/Me/2000/XP, is included with the EJ-Debug for Xtensa LX Multi Core.

Media:

CD-ROM

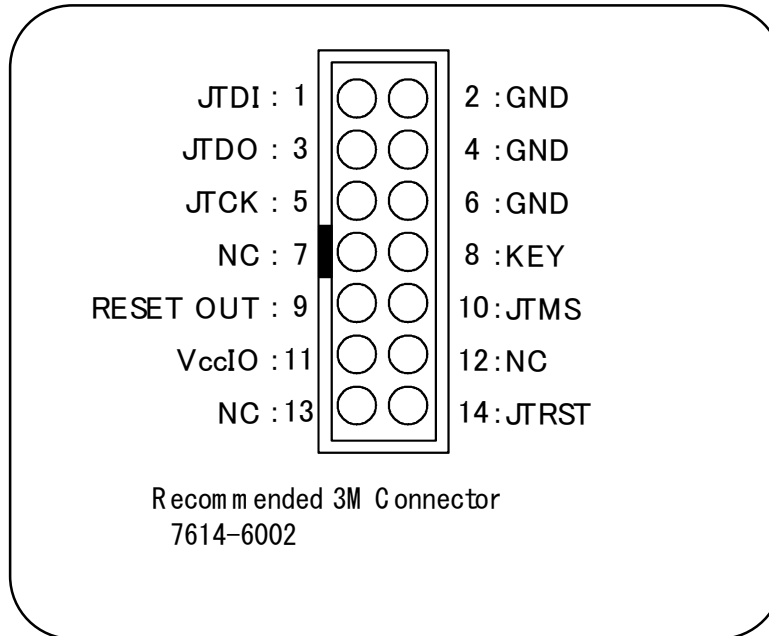
Supported Tool Chains:

Watchpoint supports the following compilers and supported OS:

Compiler:

Tensilica: C Compiler provided by Tensilica when configuring CPU.

Target ICE Connections



Ordering Information

Part No.	Description
EJD8001E	Probe Set, EJ-Debug for XtensaLX Multi Core with USB host interface and Watchpoint® debugger for Windows®98/Me/2000/XP
<Option> EJT8000E	EJD WP-TC XTENSA (required to support the trace capability)

System requirements for Watchpoint® Debugger:

OS: Windows98/Me/2000/XP **Memory:** 32 Mbyte (64 Mbyte recommended)
Hard Disk: 20 Mbyte for installation

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Windows is a registered trademark of Microsoft Corporation.

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All configurations are subject to change without notice.



Sophia Systems Co., Ltd.

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