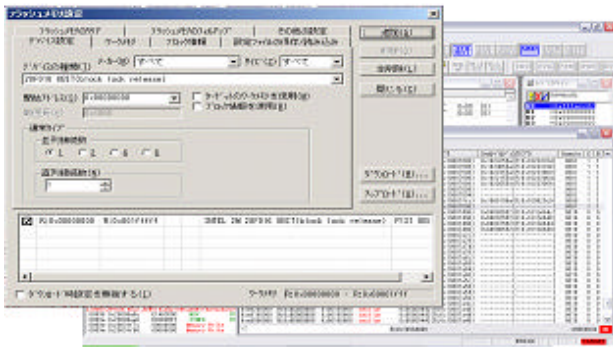


WATCHPOINT Debugger for EJ-SCT ARM MULTI CORE JTAG



- ❑ Supports ARM licensed Cortex®, ARM11®, ARM9TDMI®, ARM7TDMI®
- ❑ Multi-core debugging among the same type of CPUs is supported.
- ❑ Supports ARM's Multi-ICE interface
- ❑ CPU Equipped with automatic detecting function (JTAG Selector)
- ❑ ARM®/Thumb® state debugging support, etc. (Thumb, Thumb2, Thumb2EE, UFP, SIMD, etc.)
- ❑ Hardware breakpoints can be set for address and status conditions
- ❑ Unlimited software breakpoints (can be set for RAM and Flash ROM)
- ❑ Supports the semi-hosting capability
- ❑ Download to Flash Memory capability
- ❑ Useful for field debugging or maintenance
 - Powered by USB bus (No AC adapter required)
 - Small size (86mm X 101mm X 23mm)
- ❑ The optional ETB capability is available.
- ❑ Auto-script execution by BATCH button on the hardware unit
 - perfect use in auto-verification of the target on mass production or for updating new versions
- ❑ USB2.0 host interfaces for high-speed communication with host computer
- ❑ Sophia's high-level language debugger, WATCHPOINT® is included with all Sophia Systems emulators (Windows® 2000/XP/Vista* platforms)

Specifications

Target CPU	Cortex, ARM11, ARM9, ARM7 Cortex Core Series (A8, R4, M3) ARM11 Core Series (ARM1136, ARM1176 etc.) ARM9 Core Series (ARM9TDMI, ARM9TDMI-S, ARM910T, ARM920T, ARM940T, ARM9E, ARM946E, ARM966E, ARM922, ARM925, ARM926 etc.) ARM7 Core Series (ARM7TDMI, ARM7TDMI-S, ARM710T, ARM720T, ARM740T etc.)
Target Vcc	Vcc= +1.8 V to 3.6 V
Memory and I/O	Entire space is available to user
Interrupts	Both internal and external interrupts are available to user
Breakpoints and Break Options	<ul style="list-style-type: none"> • Hardware breakpoints <ul style="list-style-type: none"> - 2 hardware breakpoints (ARM7/ARM9) Instruction execution address, memory access, data can be specified. - 7 hardware breakpoints (ARM11): Instruction execution address (3 points), memory access (2 points), others(2 points) - 9 hardware breakpoints (Cortex R4) Instruction execution address (6 points), memory access (1 points), others(2 points) • Unlimited software breakpoints, Other break options: <ul style="list-style-type: none"> ▪ Forced break from Debug Monitor <p>Note: ARM7/9, with Software Breakpoints, Step Over, Step Out, Come to function is used, then 1 H/W breakpoint used.</p>
ETB Capability	ETB trace via JTAG for WATCHPOINT option available.
Flash Memory	1. Download a User program directly to the target's Flash memory. 2. High-speed using target area.

Configuration



CD-ROM



JTAG CABLE types:

- SCP7500: 20 to 20 pin
- CS2801: 20 to 14pin (ARM)
- VK0019 : 20 to 14pin (TI)

Supported Tool Chains:

WATCHPOINT supports the following compilers and OS:
Compiler:

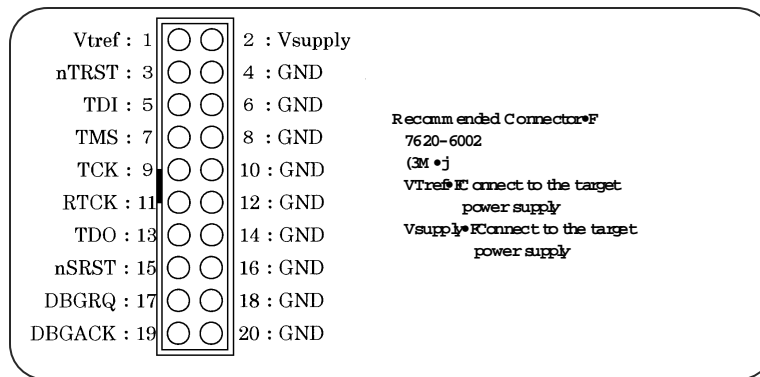
- TI Code Composer Studio®
- ARM: ADS, RealView
- Metaware: High C/C++/EC++ for ARM
- Green Hills: GHS
- GAIO: XCC-V
- GNU:
- IAR: EWARM

Supported OS:

- NORTi G-OS PrKERNEL
- VxWorks Linux iTRON
- Symbian Windows CE L4 μ-kernel

*Please contact Sophia Systems for the latest tool chain info.

Target ICE Connections



Multi ICE JTAG Header Connector
 Pin Assignment (Top View)

Ordering Information

CUSTOMER should PERPARE		Necessary items for Debugger System			Options
HOST PC	CONNECT WITH PC	JTAG EMULATOR (Hardware)	WATCHPOINT Debugger (software)	SUPPORT SERVICE (Software updates)	Optional SOFTWARE
DOS/V & NOTE PC (IBM PC/AT & COMPATIBLE MACHINE)	USB2.0/1.1 CONNECTION	SCD001 EJ-SCT	SCM0791E WP DBG for EJS ARM	SSS001 Sophia Support Service	U4A401 WP4ARMETB *Necessary for ETB trace

System requirements for WATCHPOINT® Debugger:

OS: Windows2000/XP/Vista Memory: 64 Mbytes+ recommended Hard Disk: 25 Mbytes for installation

Notes:

- * Vista (32-bit version): driver software update is required.
- * Vista (64-bit version): Contact Sophia Systems for WATCHPOINT updates.
- * XP (64-bit version): driver software update is required.
- * XP (64-bit version): operation-confirmed only with AMD's Athlon64.

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