



Cortex & ARM series: EJ-Extreme ICE ETM + JTAG + Long term trace (100GIG)



- ❑ Supports ARM licensed Cortex[®], ARM11[®], ARM9TDMI[®], ARM7TDMI[®]
- ❑ ARM[®]/Thumb[®] state debugging support, etc. (Thumb, Thumb2, Thumb2EE, UFP, SIMD, etc.)
- ❑ Hardware breakpoints can be set for address and status conditions
- ❑ Unlimited software breakpoints (can be set for RAM and Flash ROM)
- ❑ Download to Flash Memory capability
- ❑ Long Term Trace capability to record the execution data onto a HDD (hard disc drive) for longer periods of time
- ❑ ETM trace up to 200MHz clock is available
- ❑ Low voltage from 1.8V
- ❑ USB host interfaces for high-speed communication with host computer
- ❑ Sophia's high-level language debugger, WATCHPOINT[®], is included with all Sophia Systems emulators (Windows[®] 2000/XP, Vista* platforms)

Specifications

Target CPU	Cortex core series *INCLUDING all ARM licensee IC Vendors. ARM11 core series ARM9 core series (ARM9TDMI, ARM9TDMI-S, ARM910T, ARM920T, ARM9E, ARM940T, ARM946E, ARM966E, ARM922, ARM925, ARM926, etc.) ARM7 core series (ARM7TDMI, ARM7TDMI-S, ARM710T, ARM720T, ARM740T, TMS470 series, etc.)
Clock	Supports the CPU's maximum clock speed
Target Vcc	Vcc= +1.8 V to 3.6 V
Memory and I/O	Entire space is available to user
Interrupts	Both internal and external interrupts are available to user
Breakpoints and Break Options	<ul style="list-style-type: none"> ● Hardware breakpoints <ul style="list-style-type: none"> - Cortex: Pre cpu core breakpoint capabilities. - ARM11: Max 7 hardware breakpoints: Instruction execution address(3 points), memory access(2 points), others(2 points) - ARM7/ARM9: Max 2 points*: Instruction execution address, memory access, data can be specified. ● Unlimited Software breakpoints ● Other break options: Forced break from Debug Monitor <p>Note: * = In ARM7/9, when the Software Breakpoint, Step Over, Step Out, Come to function is used, then 1 H/W BP is used.</p>
ETM Trace	<p>Long Term Trace capability</p> <ul style="list-style-type: none"> ● Trace memory capacity: 2G bytes + 100G bytes HDD ● Supported clock: 200MHz (*Check with Sophia Systems about other increased speed cpu types) ● Trace memory capacity: 512K STEP (This is the capacity when Long Time Trace is not used) ● Data trace available ● ETM trigger can be specified (such as point, area, sequential, count, etc) ● ETM trigger break available ● Time stamp capability ● ETB capability (The optional Watchpoint software is required.)
Flash Memory	1.Download User program directly to the target Flash memory. 2. High-speed download via target area setup.

Configuration

Hardware

The EJ-Extreme Cortex/ARM ETM Long Time Trace Emulation System consists of the EJ-Extreme Probe Set with USB host interface.

* This product supports ARM CPU types.

Software

WATCHPOINT® high-level language Debugger for Windows®2000/XP, Vista* is included with the EJ-Extreme Hardware.

Media:

CD-ROM

Supported Tool Chains:

WATCHPOINT supports the following compilers and OS*:

Compiler:

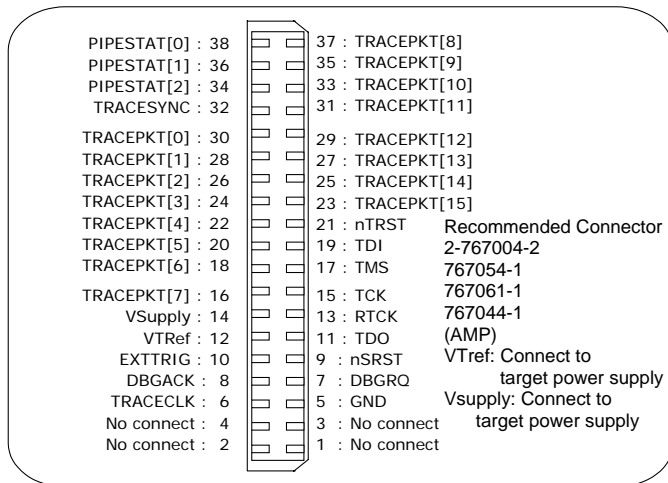
TI	Code Composer Studio®
ARM:	ADS, SDT, RVCT
Metaware:	High C/C++/EC++ for ARM
Green Hills:	GHS
GAIO:	XCC-V
GNU:	
IAR:	EWARM

Supported OS:

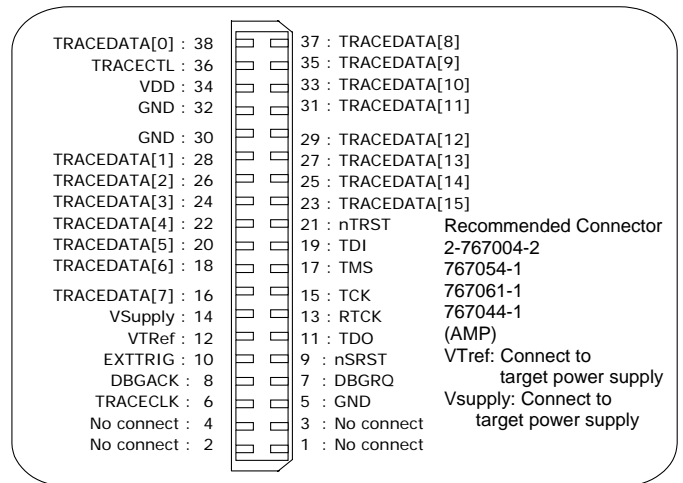
NORTi	G-OS	PrKERNEL
VxWorks™	Linux	iTRON
Symbian™	WinCE	

* Contact Sophia Systems for latest tool chain info.

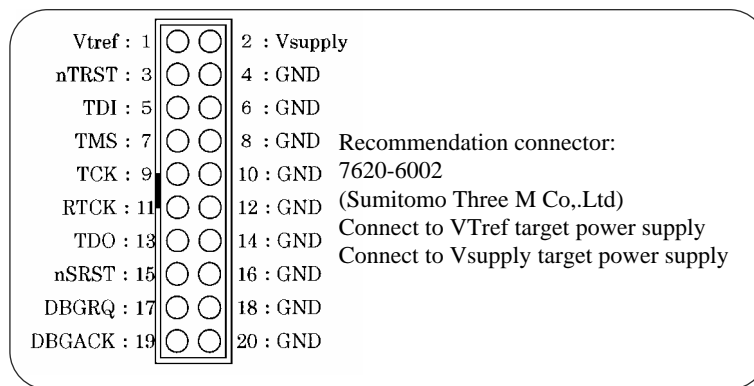
Target Connection 1



Single ETM target connector pin assignment Top View
ARM7 / ARM9



Single ETM target connector pin assignment Top View
ARM11, Cortex



JTAG Connector pins – Top View

Ordering Information

Part No. Description

AK72301E Probe Set, EJ-Extreme Cortex, ARM series -Long Term Trace with USB interface, and WATCHPOINT® Debugger.

Minimum Host System requirements for EJ-Extreme with Watchpoint Debugger:

OS: 2000/XP, Vista* Memory: 64 MB recommended Hard Disk: 25 MB

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All configurations are subject to change without notice.



Sophia Systems Co., Ltd.

URL: <http://www.sophia-systems.com>