



Cortex & ARM series: EJ-Debug JTAG Emulator



- Supports Cortex®, ARM11®, ARM9TDMI®, ARM7TDMI®
- Compatible with ARM Multi-ICE interface
- ARM® Thumb® state debugging support, etc. (Thumb, Thumb2, Thumb2EE, UFP, SIMD, etc.)
- Set hardware breakpoints on address & status
- Supports the semi-hosting capability
- Unlimited software breakpoints in RAM and Flash ROM
- Clear, read and program FLASH
- Perfect for field debugging or maintenance.
 - USB bus powered - No AC adapter required.
 - Pocket sized, 86x101x23mm
- Supports ETB capability
- JTAG pod button runs User macro scripts
 - Perfect for hardware test, small run programming and automatic field upgrades.
- Fast USB2.0 PC interface
- EJ-Debug includes WATCHPOINT® for Windows®

* Multi-core debugging available as an optional feature.

Specifications

Target CPU	<ul style="list-style-type: none"> • Cortex, ARM11, ARM9, ARM7 • TI <ul style="list-style-type: none"> :CORTEX A8 (OMAP [3410, 3420, 3430, 3440, 3503, 3515, 3525, 3530]) :ARM1136 (OMAP [2420, 2430, 2431]) :ARM926 (OMAP [17xx, 16xx, 15xx, 59xx, 1610, 1611, 1612, 1621, 1710, 5912], TMS320DM[350, 355, 6446]) :ARM7 (TMS [320, 470, etc], OMAP [DM270, 850, 7xx]) • FREESCALE <ul style="list-style-type: none"> :ARM1136 (i.MX31, i.MX31L) :ARM926 (i.MX21, i.MX21S, i.MX27) :ARM920 (i.MX1, iMXL, i.MXS) • NXP <ul style="list-style-type: none"> :ARM922T (LH7A400)
Target Vcc	Vcc=+1.8 V to 3.6 V
Memory & I/O	Entire space is available to the User.
Interrupts	Both internal and external interrupts are available to the User.
Breakpoints & Break Options	Hardware breakpoints: Cortex per cpu's capability. ARM7/ARM9: Max 2 hardware breakpoints* on instruction and memory access with specified data. ARM11: Max 7 hardware breakpoints. 3 On instruction address, 2 on the memory and 2 additional points may be specified. Unlimited software breakpoints. Debugger override forced break capability. *ARM7 & 9, Step Over, Step Out, & Run to Cursor functions uses one core H/W BP.
ETB Capability	ETB trace via JTAG for WATCHPOINT option available.
Flash Memory	1. Download a User program directly to the target's external Flash memory. 2. High-speed downloading using the target's memory resources.

Configuration

The EJ-Debug JTAG Cortex/ARM series emulator for professional quality debugging on PC & laptops.

Hardware

The EJ-Debug JTAG hardware unit consists of the Cortex and ARM series Probe Set with USB host interface. (EJ-Debug JTAG supports Cortex and ARM series CPUs)

Software

WATCHPOINT® high-level language debugger for Windows® XP/2000/Vista*, is included with the EJ-Debug JTAG hardware unit
Possible to set individual details of CPU
CPU Equipped with automatic detecting function (JTAG Selector)

Media:

CD-ROM

Supported Tool Chains:

WATCHPOINT supports the following compilers and supported OS*:

Compilers:

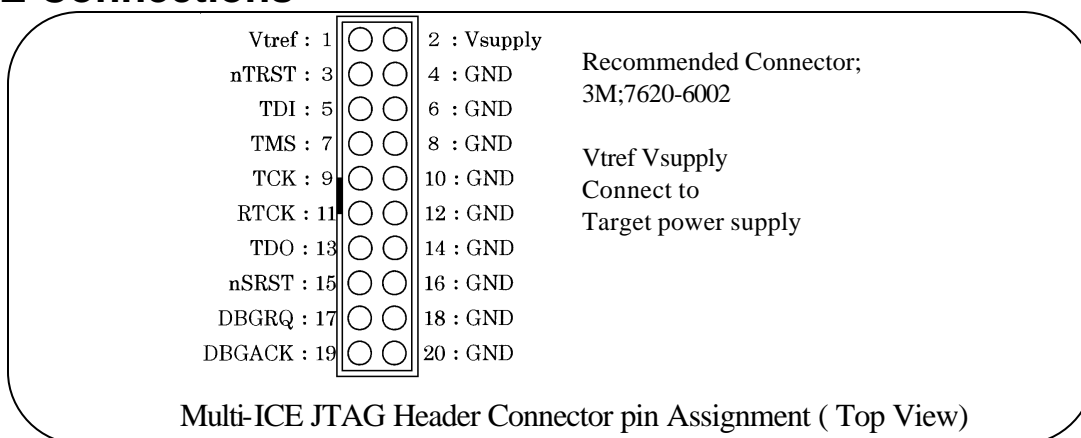
TI Code Composer Studio®
ARM: ADS, RealView
Metaware: High C/C++/EC++ for ARM
Green Hills: GHS
GAIO: XCC-V
GNU:
IAR: EWARM

Supported OS:

NORTi G-OS PrKERNEL
VxWorks Linux iTRON
Symbian Windows CE L4μ--kernel

*Please contact Sophia Systems for the latest tool chain info.

Target ICE Connections



Ordering Information

Part No.

Description

EJD7220E Probe Set, EJ-Debug for Cortex and ARM7/9/11 with USB2.0 host interface
Includes WATCHPOINT® Debugger for Windows® XP/2000/Vista*

U4A401E Optional WATCHPOINT software to support ETB trace capability via JTAG connection.

System requirements for WATCHPOINT® Debugger:

OS	Memory	Hard Disk
Windows XP/2000	64 Mbytes	25 Mbyte for installation
Windows Vista	512 Mbytes	25 Mbyte for installation

Notes:

- * Vista (32-bit version): driver software update is required.
- * Vista (64-bit version): contact Sophia Systems for WATCHPOINT updates.
- * XP (64-bit version): driver software update is required.
- * XP (64-bit version): operation-confirmed with AMD's Athlon64.

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